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Impact of Interfacial Trap Density of States on the Stability of Amorphous InGaZnO-Based Thin-Film Transistors *

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The impact of interfacial trap states on the stability of amorphous indium-gallium-zinc oxide thin film transistors is studied under positive gate bias stress. With increasing stress time, the device exhibits a large positive drift of threshold voltage while maintaining a stable sub-threshold swing and a constant field-effect mobility of channel electrons. The threshold voltage drift is explained by charge trapping at the high-density trap states near the channel/dielectric interface, which is confirmed by photo-excited charge-collection spectroscopy measurement.

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Recently, transparent oxide-based thin film transistors (TFTs) have been attracting much attention due to their potential applications in next-generation display industry. In particular, amorphous indium-gallium-zinc oxide (a-IGZO) TFTs are being extensively investigated as a replacement for the silicon-based TFTs used in active matrix displays as they could simultaneously offer high channel electron mobility, high optical transparency, low off-state leakage, and low processing temperature.[1−4] However, in spite of their promising performance, the stability and reliability of current a-IGZO TFTs is still unsatisfactory for practical applications. For example, a large threshold voltage drift upon electrical stress is commonly observed in TFTs, which would change the brightness of individual pixels and cause display non-uniformity issues. Since the electrical stabilities of a-IGZO TFTs mainly depend on the nature and density of trap states existing within the devices, it is important to study the distribution of these trap states for future process improvement.[5−7] Up to date, several methods have been applied to study the interfacial properties of oxide-based TFTs, such as photoluminescence,[8−9] deep-level transient spectroscopy,[10] gate-bias stress techniques,[11] and photo-excited charge-collection spectroscopy (PECCS).[12] Among them, PECCS is a relatively more informative characterization technique, which could quantitatively provide a density-of-states profile for deep interfacial traps in working TFTs.

In this work, the effect of trap states near the channel/dielectric interface on the stability of a-IGZO TFTs is studied under positive gate bias stress. High density interfacial trap states on the order of $\sim 10^{12}\,\mathrm{cm}^{-2}\cdot\mathrm{eV}^{-1}$ are revealed by PECCS measurement, which are believed to be the main reason for the large positive drift of threshold voltage V_{th} of the TFTs upon stress.

The back-gate a-IGZO TFTs studied in this work are fabricated on heavily doped n-type silicon substrate (see Fig. 1). A 200 nm SiO_2 gate insulator is firstly deposited by plasma-enhanced chemical vapor deposition at 300℃ on the wafer front side, which is followed by deposition of a 50 nm a-IGZO active layer by using pulsed laser deposition at room temperature in an oxygen partial pressure of 0.5 Pa. The composition of the ceramic target used is In_2O_3:Ga_2O_3:ZnO = 1:1:1 in mole ratio. The active device region is then defined by optical photolithography and wet chemical etching. Next, the source/drain contact electrodes consisting of a Ti/Au (30/70 nm) bi-layer are deposited by e-beam evaporation and are further patterned by using the lift-off technique, resulting in a device channel width/length of 100/20 μm. Finally, after deposition of the Ti/Au back-gate contact metal, the a-IGZO TFTs are annealed in air at 300℃ for one hour.

The electrical stress and current-voltage characterization are performed by using a Keithley 2636 A sourcemeter at room temperature under dark conditions. For the positive gate bias stress (PBS) experiment, the a-IGZO TFT is biased at a gate voltage of 20 V for a total time of 5000 s with both its source and drain electrodes grounded. Transfer characteristics of the device are quickly measured (<3 s)

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at selected stress time intervals. The PECCS measurement is conducted directly after the PBS stress, which has driven channel electrons to fill most interfacial trap states. As shown in the PECCS setup of Fig. 1, monochromatic light sorted by a monochromator from the output of a 500 W Xe arc lamp is directed onto the sample surface through an optical fiber. The wavelength of the incident light gradually decreases from 800 nm to 300 nm with a constant step of 5 nm. During each measurement cycle, the device under test is illuminated for 1 min by the monochromatic light and then its transfer characteristics are measured. The monochromatic light illumination is used to release trapped electrons at corresponding energy levels, which would cause a back-drift of $V_{\rm th}$. To avoid possible carrier detrapping induced by a large drain electric field, a low drain voltage of 0.1 V is applied for the transfer characteristics measurement. In addition, due to the very long electron emission time constant from deep-level traps in wide-bandgap semiconductors like a-IGZO, the thermal emission of trapped electrons in the studied energy range is negligible during the whole PECCS measurement period.

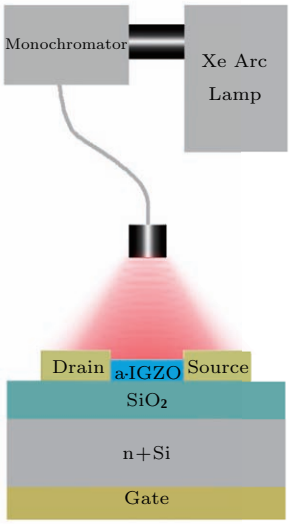

Fig. 1. Schematic of the device structure and the PECCS measurement setup.

The basic electrical properties of the fabricated a-IGZO TFTs are firstly evaluated. Based on the transfer and output characteristics shown in Fig. 2, the device works in enhancement mode with a large on-to-off current ratio ($I_{\rm on}/I_{\rm off}$) of more than 10^8. The $V_{\rm th}$ and field effect mobility ($\mu_{\rm FE}$) in saturation region ($V_{\rm DS} = 10$ V) are 2.5 V and 4.09 $\rm cm^2{\cdot}V^{-1}{\cdot}s^{-1}$, respectively, determined by linearly fitting the plot of $I_{\rm DS}^{0.5}$ versus $V_{\rm GS}$. A subthreshold swing (SS) of 0.35 V/dec is extracted from the liner portion of $\log(I_{\rm DS})$ versus $V_{\rm GS}$, suggesting that the device has a decent electrical performance.

The PBS stress is found to induce a positive parallel shift of the transfer curves (Fig. 3(a)). The amount of shift tends to saturate when the stress time is more than 3000 s, and at the stress time of 5000 s the corresponding $\Delta V_{\rm th}$ is ~6.36 V. Interestingly, in spite of the large $V_{\rm th}$ drift, the SS value of the TFT exhibits no significant change (Fig. 3(b)). Meanwhile, there is also no apparent change for $\mu_{\rm FE}$. Based on previous research, the $V_{\rm th}$ drift of a-IGZO TFTs upon PBS stress could be explained by two models: charge trapping and defect creation.[1,4,13,14] Since there is no change for SS and $\mu_{\rm FE}$ in our case, new defect generation mechanism could be excluded. Thus, the large $V_{\rm th}$ drift should be caused by the trapping of electrons, which modifies the effective electrical field induced by gate bias. In addition, since the PBS stress attracts most electrons to accumulate at the channel/gate-dielectric interface, the trapped electrons are expected to mainly stay on interfacial states.

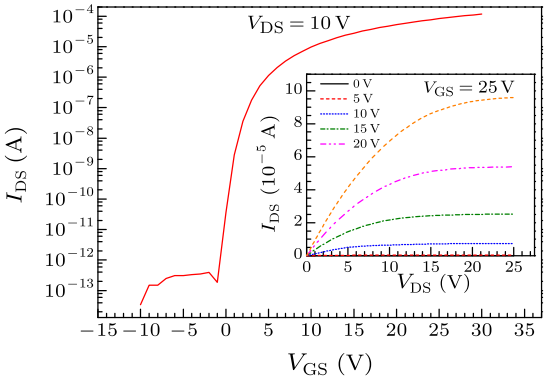

Fig. 2. Typical transfer and output curves (inset) of the a-IGZO TFT.

To investigate the nature of these interfacial trap states, the density of states (DOS) profile near the channel/dielectric interface of the a-IGZO TFT is measured by using the PECCS technique directly after the PBS stress. In the measurement, with the increasing energy of incident photons, trapped electrons from shallow to deep levels are sequentially liberated onto the conduction band of a-IGZO and then collected by the source/drain electrodes. Figure 4 shows the energy band diagram of the photo-excitation process. As a result, the formerly positively drifted $V_{\rm th}$ of the TFT would gradually drift back and the magnitude of $\Delta V_{\rm th}$ contains the DOS information of the interfacial trap states.

Figure 5(a) shows the evolution of transfer curves of the a-IGZO TFT after each monochromatic light illumination, which agrees with the physical picture of the photo-excitation process of trapped electrons. At high photon energies, the resulting transfer curves could further move to the negative side of the original transfer curve obtained before the PBS stress. It means that even without PBS stress, some deep inter-

facial traps within the a-IGZO TFT are already filled by free electrons. Based on the obtained $\Delta V_{\rm th}$ as a function of incident photon energy, the DOS profile of interfacial traps can be calculated from the equations

$$V_{\rm th}(\varepsilon) = \phi_{\rm ms} - \frac{Q_{\rm eff}(\varepsilon)}{C_{\rm ox}} + \psi_{\rm s,max} + \frac{Q_{\rm G}}{C_{\rm ox}}, \quad (1)$$

$$\frac{\partial V_{\rm th}}{\partial \varepsilon} = -\frac{1}{C_{\rm ox}} \frac{\partial Q_{\rm eff}(\varepsilon)}{\partial \varepsilon}, \quad (2)$$

$$D_{\rm it}(E_{\rm c} - \varepsilon) = \frac{C_{\rm ox}}{q} \frac{\partial V_{\rm th}(\varepsilon)}{\partial \varepsilon}, \quad (3)$$

where ε is the incident photon energy as well as the corresponding energy depth relative to the conduction band edge $E_{\rm c}$, $C_{\rm ox}$ is the capacitance per unit area, $\phi_{\rm ms}$ is the metal-semiconductor work function difference, $\psi_{\rm s,max}$ is the surface potential of the channel semiconductor, and $Q_{\rm G}$ is the gate-bias-induced interface charge. Equations (1) and (2) describe how effective interface charge ($Q_{\rm eff}$) affects $V_{\rm th}$, while Eq. (3) describes how to deduce the interfacial DOS by differentiation of $\Delta V_{\rm th}$ as a function of photon energy. A detailed explanation of the DOS analysis method has been provided in the literature.[12,15]

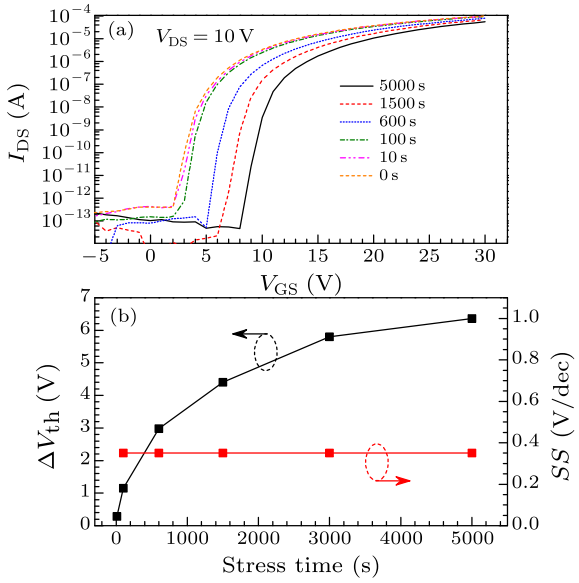

Fig. 3. (a) The transfer curves of the a-IGZO TFT after different PBS stress time. (b) The corresponding $\Delta V_{\rm th}$ and SS of the TFT as a function of stress time.

The calculated DOS profile of deep interfacial traps for the a-IGZO TFT is shown in Fig. 5(b). The DOS has an average high value of $\sim 1.5 \times 10^{12}\,{\rm cm}^{-2}\cdot{\rm eV}^{-1}$ in the energy range from $\sim$1.6 to 3.2 eV below the conduction band edge of a-IGZO, which agrees with the large $V_{\rm th}$ drift of the TFT upon PBS stress. Comparatively, it has been reported that a-IGZO TFTs with very low interfacial DOS of $\sim 10^{10}\,{\rm cm}^{-2}\cdot{\rm eV}^{-1}$ could maintain a highly stable electrical performance upon either positive or negative gate bias stress.[15,16] In addition, the DOS spectrum exhibits three distinct peaks in the energy range studied, which locate at $\sim$1.86 eV ($8.5 \times 10^{12}\,{\rm cm}^{-2}\cdot{\rm eV}^{-1}$), $\sim$2.04 eV ($2.9 \times 10^{12}\,{\rm cm}^{-2}\cdot{\rm eV}^{-1}$), and $\sim$2.43 eV ($4.0 \times 10^{12}\,{\rm cm}^{-2}\cdot{\rm eV}^{-1}$), respectively. These DOS peaks match well with the theoretical deep trap levels in bulk ZnO,[17] and could be explained as O_i(oct) (−/2−) (1.84 eV), Zn_O(4+/2+) (1.98 eV), and Zn_O(3+/2+) (2.42 eV) (here Zn_O denotes zinc antisites and O_i (oct) denotes oxygen interstitials occupying the octahedral interstitial sites). This result suggests that the interfacial trap properties of a-IGZO TFTs are similar to those of crystalline ZnO-TFTs.

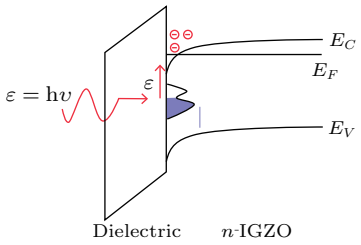

Fig. 4. Energy band diagram of the a-IGZO TFT under monochromatic light illumination.

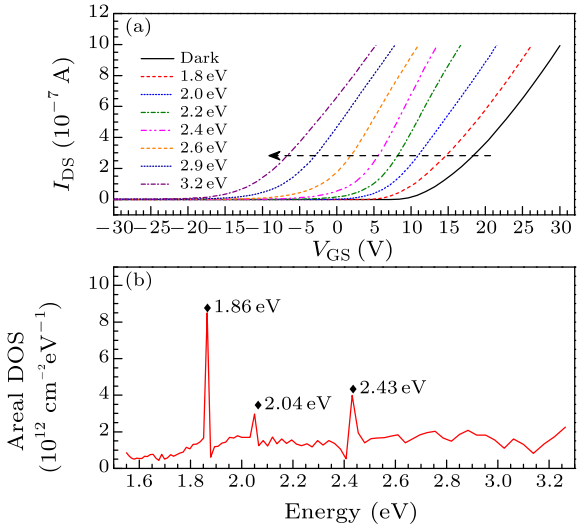

Fig. 5. (a) Evolution of transfer curves of the a-IGZO TFTs during the PECCS measurement. (b) The calculated interficial DOS profile of the a-IGZO TFT.

In summary, the effect of positive gate bias stress on the stability of a-IGZO TFTs is studied. The bias stress could induce a large positive $V_{\rm th}$ drift but has no impact on SS and $\mu_{\rm FE}$ of the TFTs. This behavior is explained by stress-induced charge trapping at the channel/gate-dielectric interface. PECCS measurement confirms that there are high density deep interfacial traps existing in the fabricated a-IGZO TFTs.

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